DER Ride-Through and Anti-Islanding Protection Advancements for Utility Engineers

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***Abstract*—With the increases in Distributed Generation, protection of the utility system has become extremely costly and complex. Classical solutions to DER(Distributed Energy Resource) islanding and fault response, such as Direct Transfer Trip(DTT), have become cumbersome for utilities to design, deploy and maintain on a large scale. Distribution and Transmission protection concerns are also further compounded by the adoption of Ride-Through requirements, which can delay tripping times for POI(Point of Interconnection) protective devices. This paper proposes alternate techniques that be used by the utility engineer to limit the amount of DTT being installed while still providing speed, selectivity and reliability of the POI protection even with Ride-Through Requirements. A Transmission/Distribution zone-selective technique is proposed that allows POI protection to differentiate between Transmission and Distribution faults, thus allowing selective high-speed tripping for Distribution events. Real-Time simulation validation and live field testing of these methods are detailed.**

***Index Terms*—DTT, Transfer Trip, Islanding, Risk of Islanding, DER, Distributed Generation, Ride Through, IEEE-1547**

I. Introduction

II. Islanding of Grid Connected DER in Electrical Utility Systems - Background

Within the utility industry, the large increase of DER penetration on the distribution system has caused a number of different problems for the protection engineer, one of which is islanding. Islanding is defined as the condition in which a DER continues to power a location even though electrical grid power is no longer present. An example of a distribution island is shown in Figure 1. In this example, a line-technician opened the feeder circuit breaker under load condition which formed a distribution island(the feeder circuit breaker at the substation is colored green indicating it is in the open position). In general, an island cannot form in a faulted state on the distribution system, and generally occurs during switching of a steady-state circuit(such as opening the feeder circuit breaker).

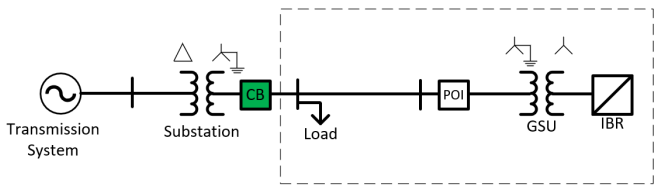

Fig. 1: Distribution Feeder Island

Islanding can be dangerous to utility workers, who may not realize that a circuit is still energized. Voltage and frequency control are absent in an island and can result in the damage of customer or utility equipment. Detecting and clearing an islanded condition is of the upmost importance for safety of electrical line workers and public safety.

While there are many technical documents available for resolving islanding concerns at the inverter level(active anti-islanding such as frequency perturbation), many of these techniques are proprietary and require time-consuming and exhaustive time-domain simulation to determine a risk-of-islanding. It is also worth noting that some anti-islanding techniques differ from manufacturer-to-manufacturer and can negatively interfere when grouped together on the same circuit, thereby reducing its effectiveness. Many utility protection engineers are left asking - what can be done at the utility distribution level to address some of these concerns? This paper proposes simple and effective techniques that can be used to identity high-risk circuits, limit the risk-of-islanding and provide faster tripping response time.

Typically, a distribution recloser a with protective relay is placed at the point of interconnection(POI) to isolate the DER from the utility in the event of a fault or island. Several basic protective techniques can be deployed to prevent an islanding condition on the distribution feeder. A simple and effective means to detect and island is to deploy a simple passive over/under voltage(27/59) and over/under(81O/U) frequency scheme. More advanced techniques can be used, such as Vector-Shift(78VS) or Rate-of-Change-of-Frequency(81R) to detect islands. All of the passive protective functions mentioned are available on most modern microprocessor protective relays. It is also worth noting that the undervoltage element does serve a dual-purpose; the undervoltage relay will trip during a fault and can also trip for a circuit island.

A. Inverter Responses to Islanded Conditions: Protection Fundamentals

Before setting any protective elements, it is important to understand how a grid connected inverter responds to an island. A detailed electrical representation of a basic distribution island from Figure 1 is show in Figure 2. Moving forward from here, it is assumed that the DER is strictly and inverter based resource(IBR).

As shown in Figure 2, the distribution circuit has been reduced to an RLC equivalent. The DER source power flow injected into the distribution system just before the island forms is represented by the variable P, while the power flow injected into the system from the utility before the island is $\Delta P + j\Delta Q$. The ΔP and ΔQ is often referred to as the power mismatch of the circuit.

At the date of the writing of this paper, most U.S. utilities require that DER maintain unity power factor. In this case,

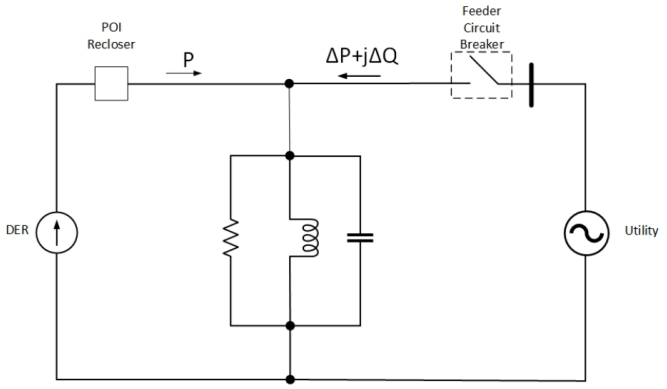

Fig. 2: Electrical Circuit of Distribution Island

for a island to form, there must be a match between the real and reactive power at the point of switching. As in the case of Figure 2, the ΔP and ΔQ mismatches will need to be sufficiently small for a protective relay not to be able to detect the island. If the mismatch values that are sufficiently small such that the POI relay cannot detect the island, this called a NDZ(non-detection zone).

A protective relay equipped 27/59/81 cannot detect an island if the power mismatches are within the following ranges:

$$Q_f\left(1-\left[\frac{f_{nom}}{f_{min}}\right]^2\right) \leq \frac{\Delta Q}{P} \leq Q_f\left(1-\left[\frac{f_{nom}}{f_{max}}\right]^2\right) \quad (1)$$

$$\left(\left[\frac{V_{nom}}{V_{min}}\right]^2-1\right) \leq \frac{\Delta P}{P} \leq \left(\left[\frac{V_{nom}}{V_{max}}\right]^2-1\right) \quad (2)$$

$$\Delta P = P_{load} - P \quad (3)$$

$$\Delta Q = Q_{load} = Q_L - Q_C \quad (4)$$

The equations in 2 and 1 represent the boundary conditions of the NDZ. If a load-flow value at the FCB is within this region, the relay element will not detect it. Since these elements are the boundary conditions, these equations can be represented graphically as shown in Figure 3. Typically, the NDZ is plotted on a parametric surface with the x-axis and y-axis representing the real and reactive power mismatch respectively.

As indicated in Equations 1 and 2, the frequency of the island will drift off-nominal if there is a VAR mismatch at the FCB(Feeder Circuit Breaker) at the time of the island. If the real power is mismatched, the voltage with drift off nominal. This is an important distinction, because this is the opposite of a rotating machine. Both real and reactive power must be matched in order to form a island that the relay cannot detect. A island that is net-capacitive will cause a under-frequency condition, while the opposite is true for a net-inductive island. If the DER is under-generating at the time of the island, ie Watts are being imported from the utility to serve load, a the voltage magnitude will decrease when the circuit breaker

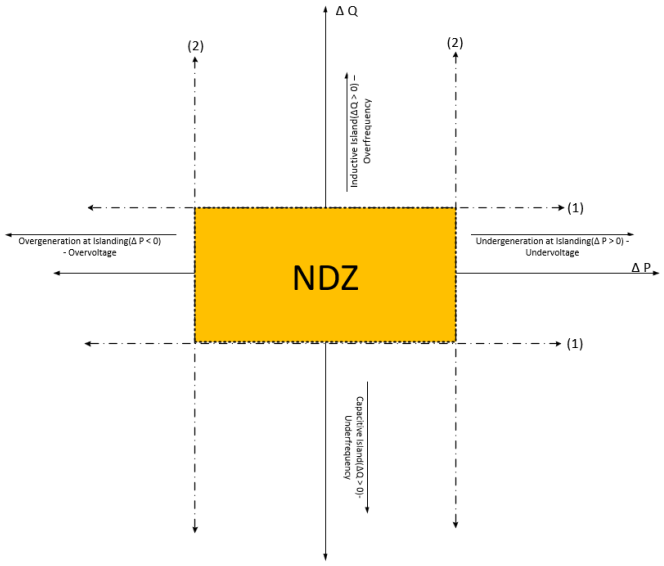

Fig. 3: Non-Detection Zone of a Distribution Island

opens to form an island. The opposite is true for a site that is over-generating, a overvoltage condition on the feeder can occur.

The quantities f_{max} and f_{min} represent the 81O/U protection set-points to detect a VAR mismatch at the circuit breaker. The V_{max} and V_{min} are the phase under-voltage 27/59 settings to detect Watt mismatch at the circuit breaker. One important variable to note is Q_f or the quality factor of the load. This quantity for an RLC circuit is a measure of its dampening. For the protection engineer concerned with islanding, this can be viewed as a "stiffness factor" to a frequency based anti-islanding algorithm or detection method. High Q-Factor circuits have large NDZs and the risk of islanding increases. A high Q-factor circuit will be stiffer and result in less frequency drift during islanding, making the island more difficult to detect.

Currently IEEE-1547 recommends and tests inverters at a $Q_f = 1$, however, this may change to 2. Studies at Power System Analytics have show that a typical feeder is usually between 0.5-0.7 and can transiently increase to 1.5-2.0 or greater. Heavy motor load circuits typically have a higher quality factor, where-as mixed residential circuit studies have shown consistently that Q_f is usually less than 1. Following IEEE guidance, a Q_f of 1 is used for most Anti-Islanding Assessments. It is worth noting that the quality factor can be estimated using field measurements. A capacitor bank switching log and feeder breaker measurements can help the protection engineer estimate the quality factor of the circuit. However, this is only a estimate. Customer loads buses may contain capacitor banks to help with power-factor correction, which appears to the utility to be a simplistic unity power-factor load.

In terms of a parallel RLC load, the quality factor Q_f is:

$$Q_f = \frac{\sqrt{Q_L \cdot Q_C}}{P_L} \quad (5)$$

The terms Q_L, Q_C and P_{load} are the reactive power absorption by the inductance, the reactive power supplied by the capacitance and the real power of the RLC load, respectively. As can be seen by Equation 5, the risk-of-islanding increases with circuits that contain a large amount of in-service capacitor banks. Conversely, if the feeder does not contain a capacitor bank, the risk of islanding substantially decreases due to the lack of a reactive power source on the feeder. However, for some utilities this may not be practical, as a capacitor bank may be place on the feeder in the future and require re-study.

B. Risk-of-Islanding Assessment:

Using the provided Equations in 1 - 5, a simple spreadsheet method can be used to determine a risk-of-islanding. Given this technique is very basic, it does illustrate to the protection engineer how "risky" a islanding event actually is.

For example, using the IEEE-1547-2003 standard settings:

- f_{min} = 57 Hz
- f_{max} = 60.8 Hz
- V_{min} = 0.88 per-unit
- V_{max} = 1.1 per-unit
- V_{nom} = 1.0 per-unit
- f_{nom} = 60.0 Hz
- Q_f = 1

The boundary conditions of $\frac{\Delta P}{P}$ and $\frac{\Delta Q}{P}$ are as follows:

$$-.108 \leq \frac{\Delta Q}{P} \leq .026 \tag{6}$$

$$-.174 \leq \frac{\Delta P}{P} \leq 0.291 \tag{7}$$

Using the boundary conditions, a specified mismatch point can be plotted to see if it resides in the NDZ. A point within the boundary conditions of the NDZ will result in a failure to detect the island if the feeder breaker were opened. If needed, the protection engineer may want to modify the OF/UF settings to reduce the risk-of-islanding. Often, using the spreadsheet method is a "iterative technique" to evaluate various conditions and settings, such as varying output of a solar PV or nightime conditions.

C. Deterministic Solutions: Direct Transfer Trip, ROCOF, Active Power Control and Other Schemes

a) Direct Transfer Trip(DTT): DTT offers many advantages and disadvantages for anti-islanding protection. A communication medium is run between the POI recloser and FCB to allow a trip signal to be transferred downstream to the DER. This design allows for nearly any anti-islanding algorithm(or none at all) to be used in the inverter with no negative consequences. Automatic reclosing coordination of the FCB is no longer an issue as DTT guarantees that the DER is removed before the breaker recloses. This can reduce the damage to customer equipment and increase the success of automatic reclosing during arcing faults.

However DTT does offer several distinct disadvantages:

1) *Cost:* DTT can be vary costly to install, both for the utility and for the DER owner. Typically most utilities will trip the POI Recloser during a communications failure. Using communication mediums such as leased-line can result in random trips of the DER recloser. Installing fiber-optic can result in a significant cost.
2) *Rigidity:* A DTT scheme is rigid by design, and a DER source cannot be moved to another circuit without blocking the scheme. During automatic switching of the system, the DER may reside on it's non-native circuit.
3) *Multiple DER:* Having multiple large DER on one feeder can be challenging for DTT schemes. A DTT network is required to pass a trip signal down the communications path to all DER on the feeder. Troubleshooting and maintaining this communications path can be costly and complex.
4) *Mid-Line Switching Devices:* If DTT is deployed on a feeder with a multiple midline device, such as a line recloser(s), this can result in a very complex DTT scheme. DTT from each recloser, plus the FCB, would be required to effectively prevent an island at any switching point on the feeder. Multiplexing of all of the trip signals is complex and cumbersome.

b) Active Power Control: NDZ Avoidance Scheme: Using Equation 2, a quick calculation can show if the active power-output of DER would result in a islanded condition if the FCB were opened(reactive power/frequency protection is not considered). Using active power control scheme, the DER output could be controlled to move the mismatch outside of the NDZ. The major advantage of this technique is that a cellular communication method could be used to transfer low-latency measurements to a control device that could place a output limit on the DER if necessary. Initial tests by the author showed that a low-bandwidth cellular channel could be used to send feeder measurements to an active-power control device.

This scheme does have a few disadvantages:

1) *Rigidity:* A NDZ avoidance scheme would also be just as rigid as a DTT scheme. The DER could not be moved to another circuit without disabling the scheme.
2) *Multiple DER:* Having multiple large DER on one feeder would result in a very complex control scheme. Attempting to deploy this type of control would prove overly complex and impractical for multiple DER feeders.

c) Vector Shift(78VS): The Vector-Shift or "Vector-Jump" algorithms monitor the phase-angle of the voltage waveform. During islanding, a sudden change in load current will cause a "jump" of the voltage phase angle, which is detected by the relay. Real-Time testing of the 78VS elements have yielded the following disadvantages:

1) *Security:* Security is a major concern of deploying the 78VS. Switching, such as capacitor banks or load may lead to repeated nuisance tripping of the element. Extensive real-time testing has shown that 78VS has been extremely difficult to secure, and nuisance tripping is extremely likely.
2) *Reliability:* The 78VS has the notable disadvantage of requiring at least a 20 percent load rejection(of the AC Rating of the DG) to operate reliably. Real-time testing has confirmed that below 20 percent, the element does

not operate reliably. As a result, the 78VS element suffers from a large NDZ.

It must be noted that what the 78VS lacks in security, it makes up for in speed. Testing of the element yielded a typical trip time of 3-5 cycles. This eliminates concerns of automatic reclosing miscoordination, lightning arrester failure, and many other concerns. However, in generally, the 78VS is not considered acceptable for most utility applications.

d) Rate-of-Change-of-Frequency ROCOF (81R): At the moment of islanding of the inverter, a small reactive power mismatch or flow at the FCB will be required to supplied by the inverter. A unity power factor constrained inverter will will respond by increasing or decreasing its frequency to a operating frequency that has no reactive power requirements. This is operating point is called a resonant frequency.

When the inverter begins to change its operating frequency due to the reactive power mismatch, the POI protection relay will sense a rate-of-change-of-frequency. As with all frequency based AI methods, high quality factor circuits can increase the NDZ of a ROCOF element. High quality factor circuits, such as heavy motor load circuits, should be approached with caution.

Extensive ROCOF testing by the author has shown that the NDZ of the ROCOF element is shaped as shown in Figure 4. The data-points plotted represent points within the NDZ of the ROCOF element. To derive this NDZ, a simple RLC test circuit was developed, and allowed to island(the exact same circuit as Figure 2). A current limited constant power inverter was added to the circuit as a source with a simple thevanin equivalent representing the utility system. A Real-Time program was allowed to perturb the RLC load, but was required to keep the quality factor the same. After the island was formed, if the protective relay(a SEL-651R in this case) did not trip, this data-point was recorded plotted in Figure 4. A ROCOF setting of 2.5Hz/s was used with a delay of 0.1 seconds.

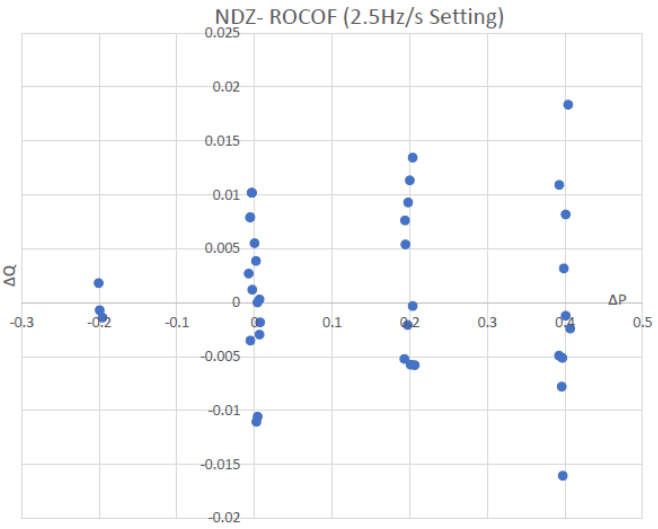

Fig. 4: Non-Detection Zone ROCOF Element with a 2.5Hz/s setting(Q_f = 1)

Upon initial inspection of the NDZ of Figure 4 it is important to note how little reactive power was required to trip the ROCOF, even in the event that the real power was exactly matched. The NDZ for ROCOF decreases with a negative ΔP(the DER is over-generating with respect to the load). For circuits that contain DER that is larger than the native feeder load, increases the effectiveness of the ROCOF method.

ROCOF, like the 81O/U elements can be adapted to a spreadsheet method. Using simple spreadsheet calculations, it becomes apparent that ROCOF does substantially reduce(or even eliminate) risk-of-islanding. However, study must be performed on the circuit to determine how effective ROCOF will be.

III. Novel 3V0 Scheme: Zero-Sequence Overvoltage Anti-Islanding Scheme

For the utility engineer, designing a deterministic anti-islanding scheme can be difficult and very costly. A typical ROI(risk-of-islanding study) performed by consultants focus on the load flow of the feeder circuit. The focus of the utility engineer and/or the consultant is often the load mismatch at the FCB. Although this information is important, one critical piece of information that is often overlooked is load imbalance. Although the mismatch may be small at the circuit breaker, indicating the risk-of-islanding is high, analyzing the imbalance at this measurement point can provide very important information.

One of the go-to tools for anti-islanding detection is frequency based methods, such as ROCOF and 81O/U. Although this method is highly effective, the quality factor does complicate matters for the protection engineer. The Q-Factor as previously described is the effective “stiffness” of the circuit to anti-islanding detection, and is often used to measure the robustness of an algorithm.

Calculation of the Q-factor of a distribution feeder can be cumbersome and time-consuming. Power factor correction on customer owned sites can adversely impact this calculations(such as capacitor banks). Even in the event that all of this data is know, the quality factor of a feeder is a constantly changing and presents a “moving target” for the protection engineer. Ideally, another method anti-islanding method is needed that can detect islands easily, but does not have a stiffness dependency such as Q-factor.

Shown in Figure 5 is the estimated Q-factor of a 23kV Feeder located in western North Carolina. Inspection of this figures shows how dynamic the Q-Factor of a circuit can be. Capacitor bank switching logs and FCB power quality meter measurements were used to calculate this plot(measurements were taken in 60 second samples).

A. 3V0 Anti-Islanding: Sequence Components Basics

Shown in Figure 2 is the simplified circuit of an islanded distribution feeder(this Figure is represented in the phase domain). If the island in Figure 2 is represented in the sequence component domain, it would be shown as Figure 6.

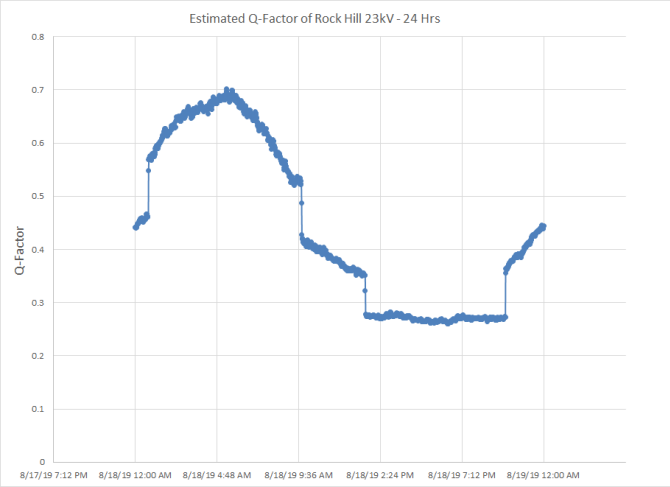

Fig. 5: Estimated Quality Factor of a Feeder over 24-hour Period

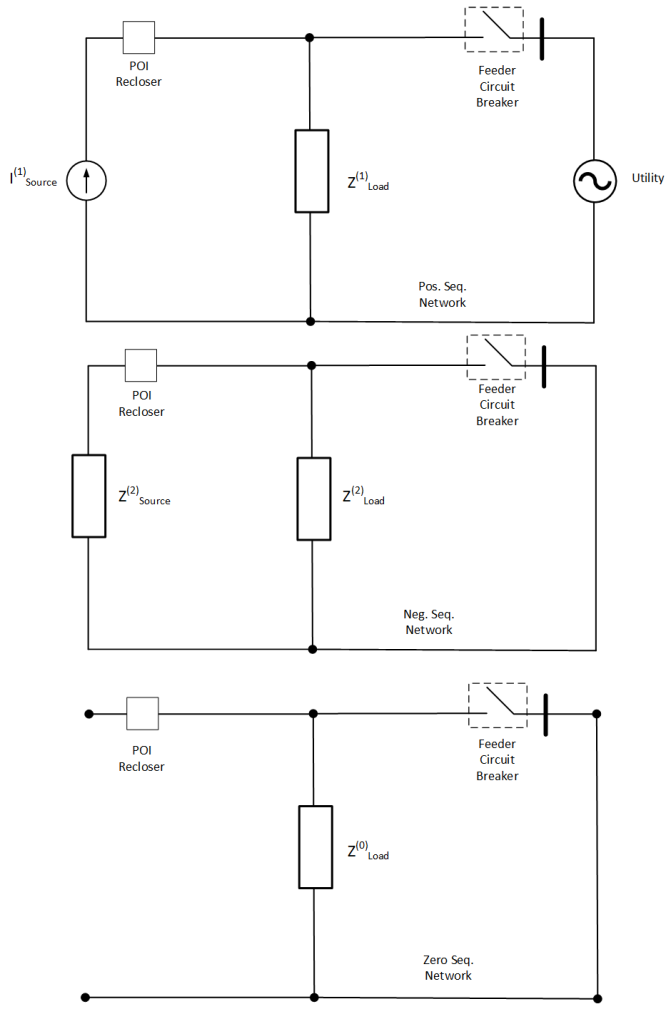

Fig. 6: Sequence Networks of Distribution Island

The IBR is represented as a constant positive sequence current source or alternatively as a constant positive sequence power source that is current limited(shown as a current source generically). This depends on the control programming of the IBR as both types are prevalent in the industry. Although ideal IBRs can be represented as pure positive sequence source, field data shows that they do allow small negative sequence currents to flow. This is represented as a high impedance or $Z^{(2)}_{Source}$ The system load in the sequence domain is show as $Z^{(x)}_{load}$. This negative sequence current can be attributed to control loop errors within the inverter.

In Figures 6 and 7, there are some assumptions that are made about the GSU step-up transformer connected to the utility system behind the POI Recloser. The transformer connection would be required to anything other than a $\Delta - Y_g$ transformer(Δ on the IBR-LV side and Y_g on the utility side). This design would insert a zero-sequence shunt impedance between POI Recloser and ground reference, thus allowing a zero sequence path other than the load on the circuit. If a alternate configuration is used, such as $Y - Y_g$, this blocks the flow of zero sequence current.

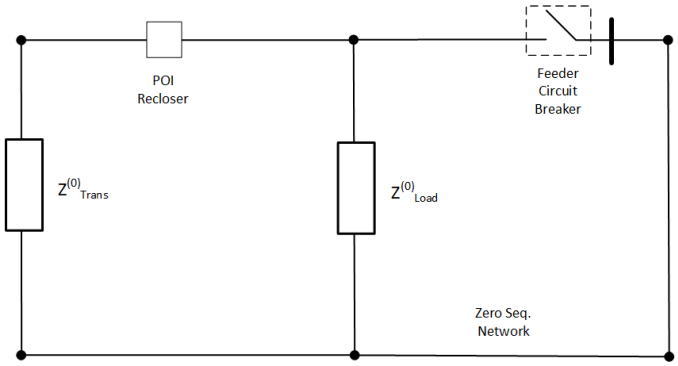

Fig. 7: Zero Sequence Network of Distribution Island with $\Delta - Y_g$ GSU transformer

As shown in Figure 6 the only path of zero sequence current is through the distribution network loads. The novel $3V^{(0)}$ anti-islanding scheme leverages the distinct advantage of sequence component coupling. Load asymmetries within the distribution island supplied by a purely positive sequence current source results in positive, negative and zero sequence voltage. With the utility source available, these sequence voltages are not present in large quantities(the utility is viewed as a nearly ideal positive sequence voltage source). As soon as the island forms, sequence coupling occurs and the zero sequence voltage will rise to a detectable level.

It is worth noting that 3-Phase/3-Limb transformers must be limited on a circuit with a $3V^{(0)}$ anti-islanding scheme. The high reluctance air-path of the zero-sequence flux will allow zero-sequence current path and reduce the effectiveness of the scheme. A 4-Limb (or higher) or three single phase transformers is considered acceptable.

B. 3V0 Voltage During Islands: Deterministic Equations

To deploy a $3V^{(0)}$ anti-islanding scheme, the load imbalance must be know or estimated. If these quantities are known, the engineer can calculate the resultant $3V^{(0)}$ seen by the POI recloser if the FCB is opened and an island occurs.

First, the sequence voltage matrix observed by the POI represented as:

$$V_s = \begin{bmatrix} V^{(0)} \\ V^{(1)} \\ V^{(2)} \end{bmatrix}$$

The sequence currents injected by the IBR observed by the POI:

$$I_s = \begin{bmatrix} I^{(0)} \\ I^{(1)} \\ I^{(2)} \end{bmatrix}$$

The sequence and per-phase impedance of the feeder load:

$$Z_{abc} = \begin{bmatrix} Z_{aa} & Z_{ab} & Z_{ac} \\ Z_{ba} & Z_{bb} & Z_{bc} \\ Z_{ca} & Z_{cb} & Z_{cc} \end{bmatrix}$$

$$Z_s = \begin{bmatrix} Z^{0} & Z^{0+} & Z^{0-} \\ Z^{+0} & Z^{+} & Z^{+-} \\ Z^{-0} & Z^{-+} & Z^{-} \end{bmatrix}$$

During the island, positive sequence current is being injected into a parallel RLC unbalanced load. Specifically, the coupling between the positive and negative sequence networks, Z^{-+} and Z^{+-}, and the coupling between the positive and zero sequence networks Z^{0+} and Z^{+0} term are now of interest. Positive sequence current injection into the unbalanced island results in a negative and zero sequence voltage buildup which is detectable by the POI relaying.

For an ideal inverter, we will assume that the IBR only sources positive sequence current, $I^{(1)}$:

$$I_s = \begin{bmatrix} 0 \\ I^{(1)} \\ 0 \end{bmatrix}$$

At this point we must make a few assumptions about the load connected to the feeder. The load must be of majority Wye grounded type. The mutual impedance can be viewed as a short circuited at a central neutral point such that:

$$Z_{ab} = Z_{ac} = Z_{ba} = Z_{bc} = Z_{ca} = Z_{cb} = 0$$

To simplify the equations, the per-phase system load(Z_{aa}, Z_{bb}, Z_{cc}) is assumed to be approximately unity PF($Z_{xx} \approx R_{xx}$) . For unity-PF controlled inverters, the system load appears to be a resonant RLC circuit. Before the island occurs, if the system load is VAR deficient(VARs are being imported by the feeder) or VAR excess(VARs are being exported by the feeder), the IBR will attempt to perturb the frequency to maintain unity PF. Therefore, we can approximate the load after islanding, as purely resistive. Even in the event that system load is off-unity power-factor, the inverter will perturb the frequency such that the load appears to be approximately resistive. In the event that the protection engineer does not desire to make this approximation, evaluation using Equation 14 and 15 can be performed.

The sequence component voltages, currents and load impedance observed by the POI recloser, V_s , I_s, and Z_s

$$[V_s] = [Z_s] \cdot [I_s] \tag{8}$$

$$[V_s] = \left([A^{-1}] \cdot [Z_{abc}] \cdot [A]\right) \cdot [I_s] \tag{9}$$

Approximating the load as resistive after the island forms:

$$|3V^{(0)}| \approx |I^{(1)}| \sqrt{R_{aa}^2 - R_{aa}(R_{bb} + R_{cc}) + R_{bb}^2 - R_{bb}R_{cc} + R_{cc}^2} \tag{10}$$

$$|3V^{(2)}| \approx |I^{(1)}| \sqrt{R_{aa}^2 - R_{aa}(R_{bb} + R_{cc}) + R_{bb}^2 - R_{bb}R_{cc} + R_{cc}^2} \tag{11}$$

$$|V^{(1)}| \approx |\cdot I^{(1)}| \frac{R_{aa} + R_{bb} + R_{cc}}{3} \tag{12}$$

For a constant current source IBR, $I^{(1)}$ can be directly plugged in at the output level of the IBR. For a constant power controlled IBR:

$$|I^{(1)}| \approx \sqrt{\frac{P^{(1)}}{Z_{aa} + Z_{bb} + Z_{cc}}} \tag{13}$$

In Equation 13, the term $I^{(1)}$ represents the positive sequence current injection into the island and the term $P^{(1)}$, is the real-power injection into the island. At full output, $P^{(1)} = P^{(1)}_{rated}$. Without approximating a resistive load the Equations 14 and 15 below can be used:

$$3V^{(0)} = I^{(1)} \cdot (Z_{aa} - \frac{Z_{bb} + Z_{cc}}{2}) + I^{(1)} \cdot (\sqrt{3} \cdot \frac{Z_{cc} - Z_{bb}}{2}) \cdot j \tag{14}$$

$$3V^{(2)} = I^{(1)} \cdot (Z_{aa} - \frac{Z_{bb} + Z_{cc}}{2}) + I^{(1)} \cdot (\sqrt{3} \cdot \frac{Z_{bb} - Z_{cc}}{2}) \cdot j \tag{15}$$

C. 3V0 Relay Security: Load v. Islands

It is important that the $3V^{(0)}$ element remain secure for normal loading imbalance conditions on the distribution network. Nuisance tripping of the POI Recloser can cause severe load rejection over-voltages(current source is being open-circuited).

Examining the sequence component voltages during the island in Equations 10 and 11, it becomes obvious that the negative and zero sequence voltages are approximately equal(assuming load impedances as purely resistive $Z_{xx} \approx R_{xx}$). This is very important for security purposes, and allows the relay to discriminate between an island and normal load conditions.

In the event that the system load is a poor power-factor load, the $3V^{(2)}$ will need to be calculated using Equation 15. Using the $3V^{(2)}$ negative sequence voltage as a permissive to increase security effectively prevents tripping of the $3V^{(0)}$ element for load conditions where the existing circuit is naturally imbalanced. However, it is good practice to capture field data or perform load flow studies to determine sequence voltage magnitudes before deploying this method. Most field

data captured has shown the $3V^{(2)}$ and $3V^{(0)}$ to be below the pickup needed for anti-islanding detection.

D. 3V0 Anti-Islanding Logic:

The anti-islanding logic for a $3V^{(0)}$ scheme can be broken into four basic parts. This is shown in Figure 8.

- 3V0-Level 1: Anti-Islanding Low-Set Level 1(Typical Setting 0.04 pu)
- 3V0-Level 2: LG/LLG Fault Detection(Typical Setting 0.5 pu)
- 27-L1: General Fault Detection(Typical Setting 0.7-0.88 pu)
- 3V2-Blocking: Negative-Sequence Voltage Blocking, Unbalanced Load Blocking
- 3V0-Delay: 3V0 Element Delay(typical setting 60-115 cyc)

The Level-1 $3V^{(0)}$ element is the anti-islanding detection for the circuit. A typical setting for this is usually 0.04-pu or higher depending on the feeder analysis. Since it is undesirable to let the $3V^{(0)}$-L1 operate for Transmission or Distribution faults(incorrect targeting), a $3V^{(0)}$ Level-2 is used to detect ground faults quickly(this is the first time we have introduced a Level-2 $3V^{(0)}$ element). Alternatively, a Level-1 under voltage can be used and is shown in the Figure. Keep in mind that the $3V^{(0)}$ is not intended to replace the undervoltage elements for anti-islanding detection, rather supplement. The region above the undervoltage level 1(0.7-0.88pu) is where the $3V^{(0)}$ anti-islanding scheme is intended to operate.

One of the more important parts of this diagram is the $3V^{(2)}$ Negative Sequence Blocking. As previously discussed, this is used to differentiate between unbalanced network load and islands. Testing using a Real-Time simulations has shown that setting the $3V^{(2)} \approx 3V^{(0)}$ is an acceptable security measure for most feeders.

The $3V^{(0)}$-L1 delay should not be set fast for anti-islanding. A setting of 60-115 cycles was found to be acceptable for a balance between security and speed. If the $3V^{(0)}$ Delay is set too fast, it is likely to operate for faults in the Distribution zone.

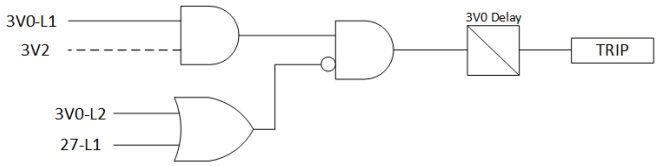

Fig. 8: 3V0 Anti-Islanding Logic Diagram

IV. Case Study: 24kV Feeder Islanding Study

To illustrate the process of evaluating a circuit for risk-of-islanding, a case study is documented in this paper. At the time of the writing of this paper, a battery energy storage system was being installed on a local utilities 24kV circuit with an output rating of 5MW. The site was required by the utility system operators to be fully operational at any time-of-day at full rated output(this is different than a standard PV farm which can only island at daylight hours). The BESS(Battery Energy Storage System) was required to operate at unity power-factor as a constant power, current-limited inverter.

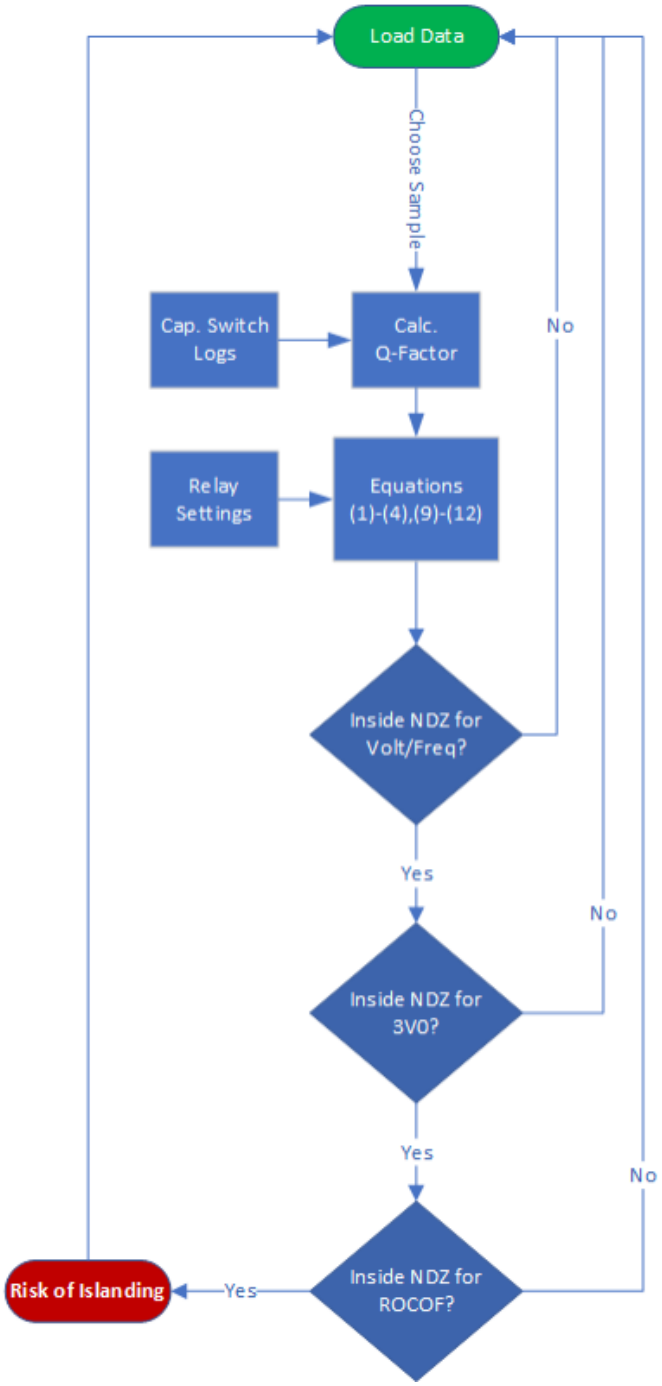

Fig. 9: Islanding Analysis Flowchart

A flowchart of the process of performing a risk-assessment is shown in Figure 9.

A. Risk Assessment: Circuit Islanding Case-Study

The studied 23kV feeder contains one 1.2MVAr capacitor bank and 1-year worth of loading data was sampled. Compared to most circuits within this utility's service territory, the feeder is fairly short at around 4.5 miles. Approximately 525,000

loading data points of Real/Reactive Power, Current, Voltage Magnitude and Power-Factor for 1-year in 60 second intervals were available measured at the Feeder Circuit Breaker.

The assumption was made that the BESS site could be active at anytime, unlike a PV plant(this can increase the risk of islanding). In the event that the engineer is performing a PV plant analysis rather than a BESS, a irradiance vs. time-of-day curve will be needed. If the BESS plant is dispatched to a set-point of power output, risk analysis can be iteratively performed also using this method to quantify total risk.

It was assumed that the feeder circuit breaker was opened on every sample and the BESS was at full rated output at the time of the islanding event. The load data between one-minute samples was assumed to be constant, and islanding was re-evaluated every sample. If an non-detectable island formed at any arbitrary sample, it was assumed to be effectively one-minute of risk.

A capacitor bank switching log was used to determine reactive power compensation and Equation 5 was used to calculate the quality factor of the circuit over one year in one-minute samples. The maximum, minimum and average estimated Q-Factor are shown below in Table I.

Q-Factor Avg.	Q-Factor Max.	Q-Factor Min.
0.4	0.7	0.2

TABLE I: Estimated Q_f of Studied Feeder over 1-year

The POI Recloser settings used to perform the analysis are shown in Table II. These settings were used in Equations 1 - 4 to determine if the system load was within the NDZ.

Parameter	Value
$P^{(1)}$	5 MW
f_{min}	57.0 Hz
f_{max}	60.8 Hz
f_{nom}	60 Hz
V_{min}	0.88 pu
V_{max}	1.1 pu
V_{nom}	1.0 pu

TABLE II: POI Relay Settings

A constant impedance load was assumed and calculated in one minute intervals using the phase-to-ground voltage measurements and line current measurements at the substation:

$$Z_{xx} = \frac{V_{LN}}{I_L} \angle \theta_{v-i} \tag{16}$$

Using the constant impedance model, Z_{aa}, Z_{bb} and Z_{cc} can be used to estimate the $3V^{(0)}$ if the FCB is opened and an island forms. Using the Equations 10 and 11, the $3V^{(0)}$ can be estimated in 60 second intervals.

Using all 525,000 data points, the $3V^{(0)}$ after a island forms was calculated. The results are shown in Table III. Notice that the average $3V^{(0)}$ during an island is around $\approx 800V$.

The number of samples of a non-detectable island for the studied feeder are shown below in Table IV. This assessment

$3V^{(0)}$ Avg.	$3V^{(0)}$ Min.	$3V^{(0)}$ Max.
850 V	4 V	3500 V

TABLE III: $3V^{(0)}$ during Islanding of Studied Feeder over 1-year

is strictly using the POI settings shown in Table II. $3V^{(0)}$ and ROCOF protection was not used to obtain Table IV.

NDZ Samples	Hr/Yr in NDZ
16,017	266.95

TABLE IV: Islanding Risk using Relay Settings in Table II without $3V^{(0)}$ and no ROCOF Protection

To illustrate the effectiveness of a $3V^{(0)}$ scheme, the same study was performed again but with ROCOF protection added(there was still no $3V^{(0)}$ protection added). A setting of 2.5 Hz/s was used with a delay of 0.1 seconds. The results of this test are shown in Table VI. The amount of time in the NDZ dropped by almost half, however, the risk was not eliminated.

NDZ Samples	Hr/Yr in NDZ
7,712	128.53

TABLE V: Islanding Risk using Relay Settings in Table II with ROCOF of 2.5 Hz/s and no $3V^{(0)}$

The same study was performed as in the previous cases with the same settings as in Table II with the proposed $3V^{(0)}$ scheme and no ROCOF protection. Notice that the amount of time in the NDZ dropped to only 6.43 hrs/yr, a major improvement over the results in Table V. This highlights the effectiveness of the $3V^{(0)}$ scheme as compared to ROCOF.

NDZ Samples	Hr/Yr in NDZ
386	6.43

TABLE VI: Islanding Risk using Relay Settings in Table II with $3V^{(0)}$ and no ROCOF

In the a final study, the settings used are exactly the same as Table II, but with the addition of a $3V^{(0)}$ setting and ROCOF combined. A $3V^{(0)}$ setting of 350V was used, along with a ROCOF setting of 2.5 Hz/s. It was determined that the solution was fully deterministic, with no islands being non-detectable by the POI relay.

NDZ Samples	Hr/Yr in NDZ
0	0

TABLE VII: Probability of Islanding using Relay Settings in Table II with $3V^{(0)}$ and 2.5 Hz/s ROCOF

The relay protection engineer may look at the results of Table IV and conclude that the result is not deterministic, and specify a Transfer Trip Scheme due to the risk. The novel $3V^{(0)}$ scheme would make the solution fully deterministic and Direct Transfer Trip would not be required.

V. Novel Transmission Ride-Through Relaying Scheme:

Ride-Through of inverters and POI relays for Transmission faults has become a very discussed topic by utility engineers. It is generically known that transmission events have caused wide-area tripping of Distribution DER(even more than 100 miles away), resulting in a large loss in distribution generation. This has caused a number of different concerns for transmission system planners around stability of the BES(bulk electric system).

Ride-Through in a generic sense is delaying of the passive protective elements to allow transmission protection to clear a fault. By delaying the passive protection on the Distribution side, the Transmission protection can clear the fault before the Distribution DER trips. This allows the Distribution DER to "ride-through" a transmission event and mitigate a wide-area loss of distribution generation.

Deploying ride-through does present a host of new problems for the utility distribution protection engineer. For example, delaying protection can cause automatic FCB reclosing overlap(the FCB opens for a fault and recloses before the POI recloser can trip), increased arc-flash hazard, increased islanding concerns and lightning arrester failure(the FCB trips with a SLG fault on the feeder will result in an overvoltage on the unfaulted phases).

Deploying a ride-through scheme does not imply compromised protection. A novel method is proposed which identifies a transmission and distribution fault. Identifying that the fault has occurred on the Transmission system is very valuable information and implies that the POI relaying should ride-through the event. Reciprocally, if the fault has occurred on Distribution there is no reason to ride-through therefore, high-speed passive elements should be allowed to operate.

A. Ride-Through: Zone Selective Protection

As previously mentioned, knowing where the fault is located(Transmission or Distribution), allows the POI relaying to respond differently for each, this is referred to as *zone selective protection*. A fault in the Transmission zone will cause the POI relay to respond differently than a Distribution fault. For example, during a Distribution fault, the POI relay does not need to ride-through and should clear as quickly as possible. However, for a Transmission event, the POI relaying must restrain and only trip after a delayed period of time(such as IEEE-1547-2018 recommendations), thus allowing Transmission relaying to respond.

A typical substation winding configuration for a Transmission to Distribution step-down transformer is a Δ - Y_g. For various fault types, the delta winding provides a substantial amount of information to the POI relay via symmetrical components and phase quantities. Using these quantities, the POI relaying can determine the location of the fault and respond appropriately.

Zone selective protection solves a substantial level of problems associated with POI ride-though. Fast tripping for Distribution faults decreases arc-flash hazard and substantially decreases the risk of lightning arrester failure during SLG faults on the feeder. Also, reclosing overlap is less of a concern due to high-speed tripping of the zone selective protective functions. *Therefore, the utility engineer can deploy the benefits ride-through without compromising protection of the distribution system.*

B. Faults: SLG Faults

The most simplistic example of fault locating using relay logic at the POI is a SLG fault. Most faults that occur on the Distribution and Transmission system are Single-Line to Ground(SLG). Lets consider a fault close into the FCB at the substation bus. The symmetrical components network for a fault on the distribution system is shown in Figure 11. If the fault is slid to the Transmission system, this is represented by Figure 10.

Looking at Figure 10, it can be seen that a fault on the Transmission system will produce no zero-sequence voltage seen by the POI Recloser $V_{POI}^{(0)}$. *A transmission SLG fault will not produce zero-sequence voltage on the distribution system. This inherently has the feature of being a fault locator.*

Notice that in Figure 11, the zero-sequence voltage observed by the POI recloser is substantial. Both the Transmission system and IBR inject fault current through the substation transformer zero sequence impedance, $Z_T^{(0)}$, which impresses a large zero sequence voltage across the POI recloser. This is easily detectable as a Distribution fault. Therefore, we can set a "fast" $3V^{(0)}$ zero-sequence over-voltage element to trip for SLG Faults on the Distribution System. We previously referred to this as a Level-2 $3V^{(0)}$.

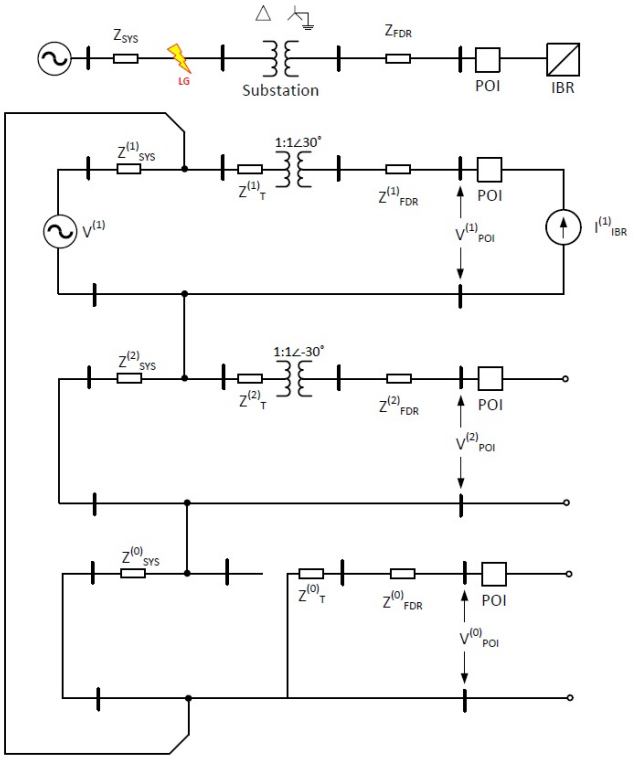

Fig. 10: Symmetrical Components Representation of Line-to-Ground Fault on Transmission System

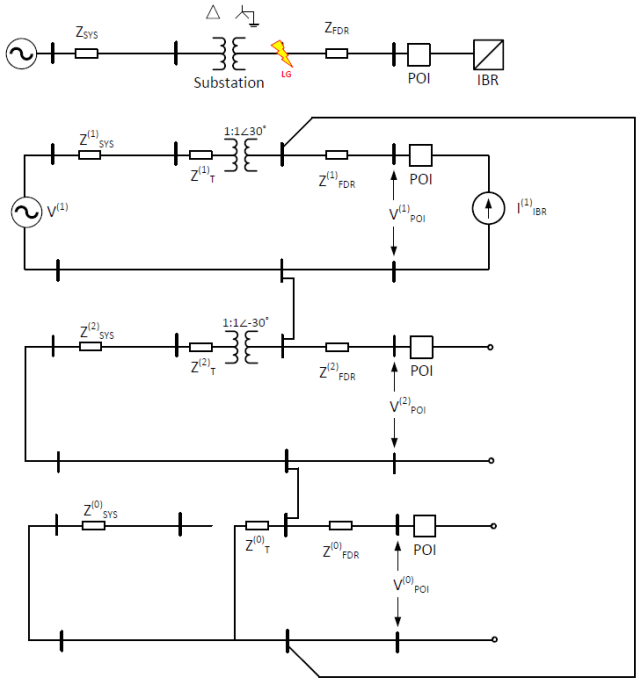

Fig. 11: Symmetrical Components Representation of Line-to-Ground Fault on Distribution System

Short-circuit analysis shows that for a typical bolted SLG fault, the zero-sequence $3V^{(0)}$ voltage observed by the POI relay is approximately the pre-fault Line-to-Ground voltage. A $3V^{(0)}$ element that is set to 0.5pu(on a line-to-ground base) would allow the POI relaying to be selective for SLG distribution system faults only(it should be set much higher than the natural $3V^{(0)}$ load imbalance). Using a set-point of 50% of the rated line-to-ground voltage offers a setting that is both selective and secure.

The delay can be set significantly faster than the ride-through since it is known the fault is on the distribution system. A typical delay of this element would be around 4.5-10 cyc. A setting value of 5 cycles was recently field deployed with very good results.

It is important to note here that there are two $3V^{(0)}$ elements are active. One is for SLG fault detection and the other is for islanding detection. The fault detection is set much higher and faster than the islanding detection.

C. Faults: LLG Faults

LLG faults are detectable in the same fashion as a LG fault. Although the sequence network is not shown in this paper, the positive, negative and zero-sequence networks are in parallel(rather than in series for the LG case).

Analyzing the sequence network for a LLG case yields the same results as in the LG case. A large zero-sequence voltage is observable by the POI recloser for Distribution faults and there is no zero sequence voltage when the fault is on the Transmission side. A setting of 0.5 pu for both LG and LLG cases for fault detection on the Distribution network has been shown to work for both cases.

D. Faults: LL Faults

Line-to-Line faults are the second most difficult fault to locate. There is no zero-sequence voltage generated for a Transmission or Distribution LL fault. This directly implies that we have lost the advantage of using zero sequence voltage blocking properties of the $\Delta - Yg$ substation transformer. A more detailed analysis is needed of a Line-to-Line fault to observe if there are distinguishable properties of a Transmission vs Distribution fault.

Two solutions are presented in this section of the paper for locating phase-to-phase faults. The first solution involves using only the phase-domain(phase voltages) to locate the fault, and the other uses symmetrical components. Multiple solutions are presented in this paper as the protective relaying used by the engineer may not allow for complex arithmetic using sequence components.

1) Solution 1: LL Fault in Phase Domain: Starting with the sequence component diagram in Figure 12, we can see that a LL (B-C specifically) fault has occurred on the Distribution system close into the substation bus. To simplify our analysis, we can neglect the fault current contribution from the IBR as it is minimal relative to Transmission system. Also, it is assumed that the negative and positive sequence impedances are equal for the substation transformer and transmission system: $Z_{sys}^{(1)} \approx Z_{sys}^{(2)}$ and $Z_T^{(1)} \approx Z_T^{(2)}$.

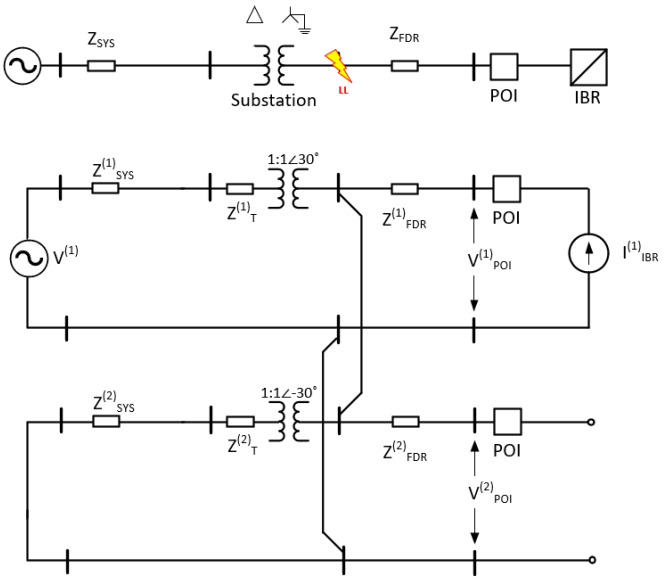

Fig. 12: Symmetrical Components Representation of a Line-to-Line Fault on Distribution System

Although the derivation is not shown here, for this case, the line-to-ground and line-to-line voltages observed by the POI recloser during the Distribution fault in Figure 12 are:

$$\begin{bmatrix} V_{ag} \\ V_{bg} \\ V_{cg} \end{bmatrix} = \begin{bmatrix} V^{(1)} \\ -\frac{V^{(1)}}{2} \\ -\frac{V^{(1)}}{2} \end{bmatrix}$$

$$\begin{bmatrix} V_{ab} \\ V_{bc} \\ V_{ca} \end{bmatrix} = \begin{bmatrix} \frac{3}{2} \cdot V^{(1)} \\ 0 \\ -\frac{3}{2} \cdot V^{(1)} \end{bmatrix} \Bigg|_{V^{(1)}=\frac{V_{LL}}{\sqrt{3}}} = \begin{bmatrix} \frac{\sqrt{3}}{2} \cdot V_{LL} \\ 0 \\ -\frac{\sqrt{3}}{2} \cdot V_{LL} \end{bmatrix} \quad (17)$$

If we move the same fault to the Transmission system (HV side of the transformer onto the Transmission Line), the line-to-ground and line-to-line voltages observed by the POI recloser during the fault are:

$$\begin{bmatrix} V_{ag} \\ V_{bg} \\ V_{cg} \end{bmatrix} = \begin{bmatrix} \frac{\sqrt{3}}{2} \cdot V^{(1)} \\ 0 \\ -\frac{\sqrt{3}}{2} \cdot V^{(1)} \end{bmatrix}$$

$$\begin{bmatrix} V_{ab} \\ V_{bc} \\ V_{ca} \end{bmatrix} = \begin{bmatrix} \frac{V_{LL}}{2} \angle 120^\circ \\ \frac{V_{LL}}{2} \angle -60^\circ \\ V_{LL} \angle 120^\circ \end{bmatrix} \quad (18)$$

Using the Line-to-Line voltages during the fault in Equations 17 and 18, we can show that only a Distribution fault can yield a Line-to-Line voltage of approximately 0 on the distribution side. This is a unique signature of a Line-to-Line fault on the distribution system. For a fault on the Transmission side, the magnitude of the Line-to-Line voltage can only depress to 0.5 per unit on a line-to-line voltage base.

Fault Type	Line-to-Line Measurements
L-L Trans. Fault(B-C)	$\lvert V_{ab}\rvert = \frac{V_{LL}}{2}$ $\lvert V_{bc}\rvert = \frac{V_{LL}}{2}$ $\lvert V_{ca}\rvert = V_{LL}$
L-L Dist. Fault(B-C)	$\lvert V_{ab}\rvert = \frac{\sqrt{3}}{2} \cdot V_{LL}$ $\lvert V_{bc}\rvert = 0$ $\lvert V_{ca}\rvert = \frac{\sqrt{3}}{2} \cdot V_{LL}$
L-L-G Trans. Fault(B-C-G)	$\lvert V_{ab}\rvert = \frac{V_{LL}}{3}$ $\lvert V_{bc}\rvert = \frac{V_{LL}}{3}$ $\lvert V_{ca}\rvert = \frac{2}{3} \cdot V_{LL}$
L-G Trans. Fault(A-G)	$\lvert V_{ab}\rvert = \frac{\sqrt{7}}{3} \cdot V_{LL}$ $\lvert V_{bc}\rvert = \frac{\sqrt{7}}{3} \cdot V_{LL}$ $\lvert V_{ca}\rvert = \frac{V_{LL}}{3}$

TABLE VIII: Fault Types and Line-to-Line Voltages observed at POI relays(B-C Fault)

A protection engineer is likely to investigate other fault types(LG, LLG) on the Transmission system to observe the results. Although the derivations are not shown here, the Line-to-Line Voltages of the POI recloser for various fault types are shown in Table VIII.

Notice that the lowest voltage for a Transmission fault of any type is approximately 0.33 per-unit on a Line-to-Line base. A Distribution Line-to-Line fault is the only fault type that depresses the voltage to less than 0.33 per unit. Using this information, relay logic can be used to correctly identify a Line-to-Line Distribution fault. Using Table VIII, we can build the fault detection logic in Figure 13. A $V_{bc} < 0.33$ pu is most certainly indicative of a LL fault on the Distribution system. Also, we can also check to see if the other two measurments, V_{ab} and V_{ca} are above a 0.5 per-unit. This also rules out a LG, LLG and LL Transmission event, keeping the fault detection secure.

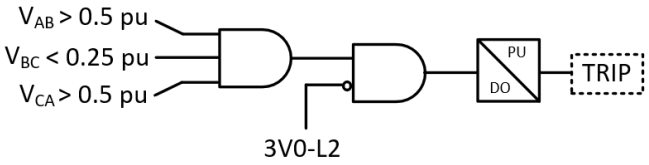

Fig. 13: High Speed Line-to-Line Fault Detection for Distribution Faults(B-to-C Phase Only)

The last check of the logic is zero-sequence voltage. For any Transmission fault event there should be no zero-sequence voltage observed by the POI. Therefore, a $3V^{(0)}$ Level-2 element is added. This element was used in the LG fault section to identify LG events on the distribution system and was recommended to be set at around 0.5 per-unit on a line-to-ground base. In the event that the $3V^{(0)}$ Level-2 element picks up during the detection process, the element is immediately blocked. A typical setting for the L-L detection pickup(PU as shown in Figure 13) is around 4.5-10 cycles.

2) Solution 2: LL Faults in Sequence Domain(Novel Sequence b0 Ratio Method): During a Line-to-Ground fault, the $\Delta - Y_g$ substation transformer offers the known advantage of not reflecting a zero-sequence voltage from the primary to the secondary. However, negative and positive sequence voltage are reflected through the winding making the sequence component fault locating for LL faults non-trivial.

If we begin using Figure 12 with a B-C fault on the Transmission network close into the substation transformer(Figure 12 shows a Distribution fault, this example slides the same fault to the Transmission Line). As before, we will neglect the contribution of the IBR due to the relative weak short-circuit response relative to the transmission system. We also again assume that $Z_{sys}^{(1)} \approx Z_{sys}^{(2)}$ and $Z_T^{(1)} \approx Z_T^{(2)}$. Also, since the system impedance and substation transformer negative/positive sequence impedance are in series, an equivalence of $Z_{eq}^{(1)} = Z_{sys}^{(1)} + Z_T^{(1)}$ and $Z_{eq}^{(2)} = Z_{sys}^{(2)} + Z_T^{(2)}$.

Using the above equivalency, the derivation of the POI sequence voltages can be shown to be:

$$V_{poi}^{(1)} = Z_{eq}^{(2)} \cdot \frac{V^{(1)}}{Z_{eq}^{(1)} + Z_{eq}^{(2)}} \cdot (1\angle 30^\circ) \quad (19)$$

$$V_{poi}^{(2)} = Z_{eq}^{(2)} \cdot \frac{V^{(1)}}{Z_{eq}^{(1)} + Z_{eq}^{(2)}} \cdot (1\angle -30^\circ) \quad (20)$$

Reducing Equation 19 and 20 using $Z_{eq}^{(1)} \approx Z_{eq}^{(2)}$:

$$V_{poi}^{(1)} = \frac{V^{(1)}}{2} \cdot (1\angle 30^\circ) \quad (21)$$

$$V_{poi}^{(2)} = \frac{V^{(1)}}{2} \cdot (1\angle -30°) \tag{22}$$

If we divide the negative and positive sequence voltages observed at the POI during the Transmission fault this is defined as the b0 ratio:

$$b0 = \frac{V_{poi}^{(2)}}{V_{poi}^{(1)}} = 1\angle -60° \tag{23}$$

If we perform the same fault on the Distribution network as it shown in Figure 12:

$$b0 = \frac{V_{poi}^{(2)}}{V_{poi}^{(1)}} = 1\angle 0° \tag{24}$$

Although it is beyond the scope of this paper, the sequence ratio voltage, b0, can be derived for all fault types in the Distribution and Transmission zone as shown in Table IX.

Fault Type	b0(Delta Lag 30°)	b0(Delta Lead 30°)
L-L Trans. Fault	A-B = 1 ∠-180°	1 ∠-60°
	B-C = 1 ∠-60°	1 ∠60°
	C-A = 1 ∠60°	1 ∠-180°
L-L Dist. Fault	A-B = 1 ∠-120°	1 ∠-120°
	B-C = 1 ∠0°	1 ∠0°
	C-A = 1 ∠120°	1 ∠120°
L-L-G Trans. Fault	A-B = 1 ∠-180°	1 ∠-60°
	B-C = 1 ∠-60°	1 ∠60°
	C-A = 1 ∠60°	1 ∠-180°
L-G Trans. Fault	A-B = 0.5 ∠120°	0.5 ∠-120°
	B-C = 0.5 ∠-120°	0.5 ∠0°
	C-A = 0.5 ∠0°	0.5 ∠120°

TABLE IX: Fault Types and b0 sequence ratios

To utilize Table IX as a fault locator, the magnitude and angle of the b0 ratios can be examined. Notice that a Line-to-Line Distribution fault is the only fault that produces a $b0 > 0.5$ at an angle of $\pm 120°$ or $0°$. To put this into practical logic to be programmed into a relay Figure 16 has been developed as a pseudo-logic representation.

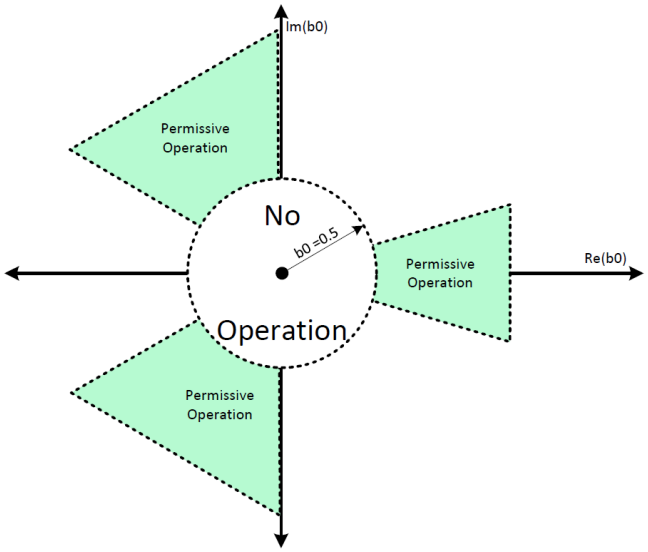

Fig. 14: b0 Plane

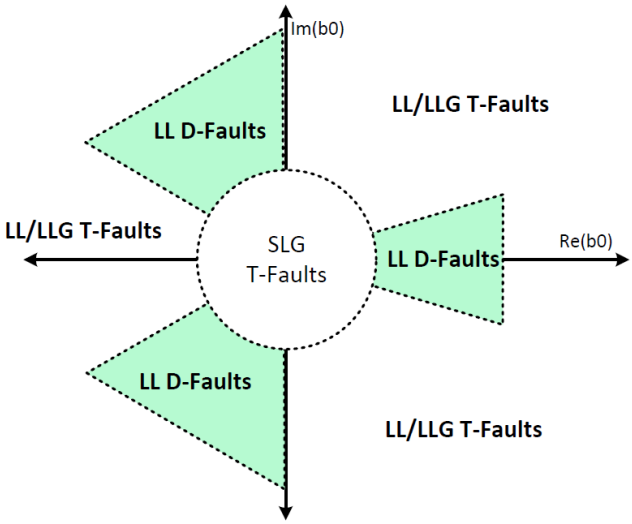

Fig. 15: b0 Fault Plane with various fault types

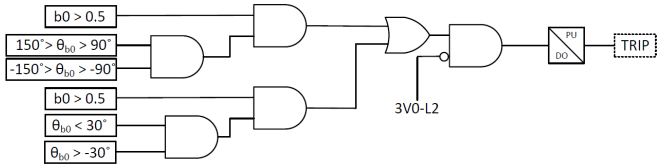

Fig. 16: b0 Fault Locating Logic Diagram

E. Faults: 3P Faults

The last fault type that has not been discussed is a 3P fault. Although 3P faults are the rarest type, it is not uncommon for a fault to begin as a LG fault and evolve to a 3P fault. Three-phase faults are very problematic for a POI relay to detect where it is located. Very little data and distinguishable features are evident for Transmission and Distribution faults.

Specific testing was done around this using various techniques such as load encroachment(positive sequence apparent impedance) with moderate success. However, it was immediately obvious during real-time simulations that 3P fault locating, no matter what was tried, was not secure. Transmission faults on the same local bus/line caused inherent security issues. Also, exact positive sequence line impedance, transformer impedance and other quantities would be required in great detail. Using various methods it was determined that 3P fault locating cannot happen without compromising security of the POI relay.

However, it must be noted that evolving faults on the Distribution system are detectable. Setting the $3V^{(0)}$ Level-2 and LL fault detection pickup faster improves the probability that an evolving fault will be detected before the transition to a 3P fault.

VI. Real-Time Testing: Inverter Controls in the Loop

Before field deployment of any relay setting or philosophy, it is important that it is laboratory verified. Until this point in the paper we have discussed only theory and case studies with no proof-of-concept. This leads to many questions that a protection engineer may ask: Does the setting and logic operate as intended? Is the relaying secure and selective? Does the relay setting meet our design criterion? What type of testing validates our settings?

Real-time Hardware-in-the-Loop(HIL) testing is considered to be the industry standard of protection testing and validation. Actual hardware, including protective relays, inverter controls and other circuit devices are connected to a HIL test-bed to provide real-time signals to each of the circuit devices. Models in software of the feeder and loads run in real-time(including the Transmission and Distribution System), allowing the protection engineer to test a variety of different scenarios such as islanding, ride-through and fault response. It is important to distinguish that during islanding and faults in this section, that the actual inverter controls are being used. No modelling of the control loops and/or proprietary anti-islanding algorithms are required. The inverter controls are controlling a software modelled power stage and plant. Therefore, the behavior observed during this testing should closely match field behavior of the IBR.

A. Real-Time Testing: Preliminary Study, Testing Conditions and Setup

A local utility case study was chosen on a 24kV circuit with a 5MW BESS undergoing a feasibility and protection study. The same circuit previously studied in Section IV(Case Study 23kV Feeder Islanding Study) was again considered. Circuit conditions including load, quality factor and other parameters were kept the same in both the previous case study and Real-Time validation testing. The only parameters that were changed for Real-Time testing in this section were the POI relay settings. Notice that the passive POI settings are now IEEE-1547-2018 ride-through compliant.

To perform the HIL testing, a Typhoon HIL test-bed was chosen for its ease of setup and detailed software modelling of utility feeder devices(such as loads, transformers and lines). A SEL-651R recloser control relay was chosen as the POI protective relay in addition to a 5MW BESS EPC Power Inverter Controller.

As with the previous case study presented earlier, the flowchart in Figure 9, a preliminary study was done by looking at the load data, Q-Factor and Capacitor Bank switching logs. The BESS was also required to be dispatchable to full-rated output at anytime(this is distinctly different than a PV, which cannot generate at night).

Parameter/Setting	Value	Delay
$P^{(1)}$	5MW	
V_{nom}	24kV	
81U	f $\leq$ 58.0 Hz	300 sec.
81U	f $\leq$ 56.5 Hz	0.16 sec.
81O	f $\geq$ 61.2 Hz	300 sec.
81O	f $\geq$ 62 Hz	0.16 sec.
27	$\|V\| \leq 0.7$ pu	2.0 sec.
27	$\|V\| \leq 0.45$ pu	0.16 sec.
59	$\|V\| \geq 1.1$ pu	2.0 sec.
59	$\|V\| \geq 1.2$ pu	0.16 sec.
ROCOF	$\frac{df}{dt}$ = 2.5 Hz/s	0.1 sec.
$3V^{(0)}$-L1	V = 350 V	1.0 sec.
$3V^{(2)}$(Blocking)	V = 350 V	-
$3V^{(0)}$-L2	V = 7000 V	.075 sec.

TABLE X: POI Relay Settings

NDZ Samples	Hr/Yr in NDZ
12,331	205.51

TABLE XI: Probability of Islanding using Relay Settings in Table X without $3V^{(0)}$ and no ROCOF

The NDZ risk is shown in Table XI and was calculated using the methods used previously in Section IV. Looking at the data,it becomes immediately obvious that there are several key issues. The feeder being studied was running at a very high power factor (≥ 0.97) during most of the year, which presents a major challenge for any frequency based protection. VAR deficiencies or excess will cause the frequency to perturb from nominal thus acting as an anti-islanding aid. However, given the relatively high power factor of this circuit, the VAR flow from the substation bus to the Distribution feeder was minimal. When comparing Table XI and IV, the risk of islanding actually decreased going to Ride-Through. The reason this is the case is due to the fact that the under-frequency setting moved from 57 Hz to 58 Hz(net capacitive islands cause the system frequency to drop). Upon closer inspection, the feeder exports VARs to the Transmission system nearly 1/3 of the year.

Also, it is worth noting that the changes in the 27/59 element did not decrease risk significantly. Only small changes in the amount of hr/yr we observed even when the of the 27 undervoltage was raised to 0.88 pu. It was immediately obvious that a supplemental protective technique was needed such as ROCOF or novel $3V^{(0)}$ proposed in this paper.

B. Real-Time Testing: Testing Setup Overview

To begin, a simple model of the test feeder using field data was built in the Typhoon HIL test-bed software. The real-time model used was a simplified feeder containing a 3-Phase parallel RLC load, a substation $\Delta - Yg$ substation transformer and a 5MW BESS.

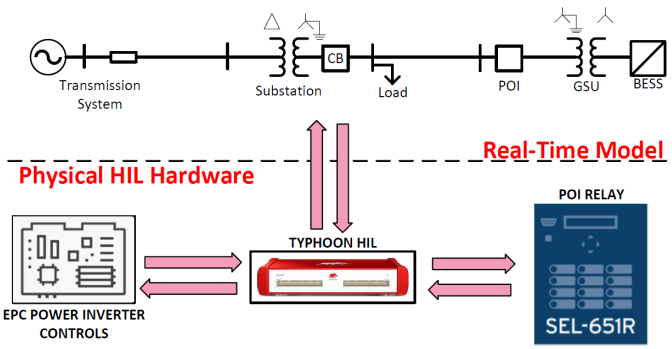

Fig. 17: Real-Time Testbed Setup

The BESS model consisted of a DC/AC power stage(3 Arm Inverter) that is controlled by a EPC Power Inverter Controls. As shown in Figure 17, the BESS is connected to a $Y_g - Y$ GSU transformer(24kV/480V). As with most utilities, the inverter controls were constrained to unity power-factor while exporting. The Inverter controls were required to maintain unity power factor and act as a constant power/current limited source. Also, the active anti-islanding in the inverter controller was disabled.

A simple circuit breaker was placed at the output of the BESS to act as the POI in the real-time model. For protection a SEL-651R-2 was chosen using R410 firmware. The relay was programmed using the Ride-Through Protection Settings in Table X. The proposed logic shown in Figure 13 for high-speed line-to-line fault detection and Figure 8 for anti-islanding detection.

C. Real-Time Testing: Testing Results

To test the novel the novel $3V^{(0)}$ scheme, the data-set of load values was filtered for high-risk loading. Using Equations 1 and 2 all 525,000 data points were filtered to identify high-risk load points.

Once all of these points are filtered and determined to be within the NDZ of the 27/59 and 81O/81U settings in Table X, the remaining data-set was further filtered. A ROCOF filter was run to examine the remaining data points to determine which points were within the NDZ of a ROCOF element of 2.5Hz/s (0.1s time-delay). The remaining loading points were calculated to be non-detectable by under-voltage, over-voltage, over-frequency, under-frequency and ROCOF.

To verify the validity of our filtering and NDZ calculations, 500 data points were selected for simulation on the real-time test-bed to ensure that none of the elements in Table X operated unexpectedly. The $3V^{(0)}$-L1 element was disabled and only 27, 59, 81O/U and ROCOF were in-service and allowed to operate. If the data-point filtering were done incorrectly, the Typhoon HIL would record a POI Relay trip implying that the data-point was not in the NDZ as calculated. Conversely, if all of the data-points were in the NDZ, a sustained island should form and be non-detectable by the SEL-651R. All 500 test-points were run with no trips occurring with the over-voltage, under-voltage, over-frequency, under-frequency or ROCOF. This validates the NDZ Equations in 1, 2, and also allows a direct measurement of the effectiveness of the novel $3V^{(0)}$ method.

Samples	Novel $3V^{(0)}$ % Success Rate
500	97%

TABLE XII: Novel $3V^{(0)}$ Method Success Rate using Real-Time HIL Tests

The success rate of the novel $3V^{(0)}$ method shown in Table XII. The test results show the scheme is very effective at detecting unintentional islands that are difficult to detect, even with ROCOF. There were 15 cases where the scheme failed to detect an island, and the island sustained indefinitely. These points were reviewed and it was determined that the $3V^{(0)}$ scheme did detect the island, however, the element began to "chatter"(repeated pickup/dropout of the element) and did not trip. The zero-sequence voltage of the island was very close to the $3V^{(0)}$ pickup level resulting in a cyclic pickup/reset of the element.

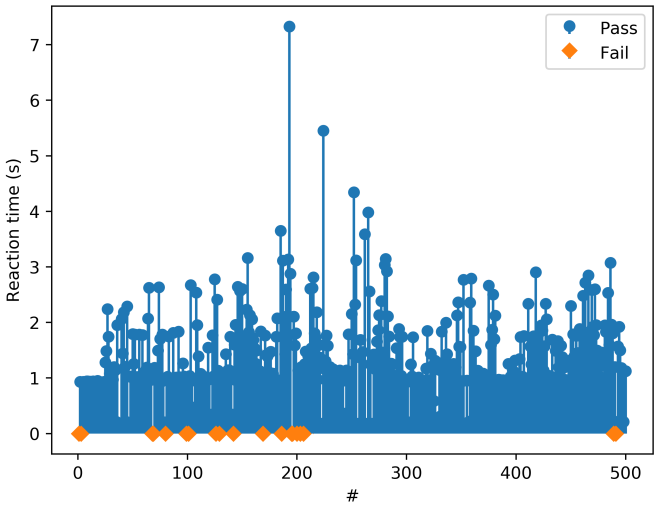

Fig. 18: Novel $3V^{(0)}$ Reaction Time(Timer Setting 1.0 Sec)

Its important to note that the $3V^{(0)}$ during the islanding event measured at the POI was compared against the calculated values proposed in Equations 14 and 15. It was found that the HIL simulations were within a maximum of $\pm 3\%$ of the calculated values.

One noticeable disadvantage that was not expected was the operate time of the $3V^{(0)}$ element as shown in Figure 18. The scheme in several instances, despite being set at a 60 cycle delay, detected the island at >2 seconds. It was noticed that there were several events lasting greater than 4 seconds, even one at nearly 7 seconds. Further investigation into the addition of a smoothing timer to prevent chattering has shown promising results to mitigate delayed tripping.

VII. Field Testing: 5MW BESS Transmission and Distribution Fault Events

After performing the Real-Time testing in the previous section with satisfactory results, it was decided to test the

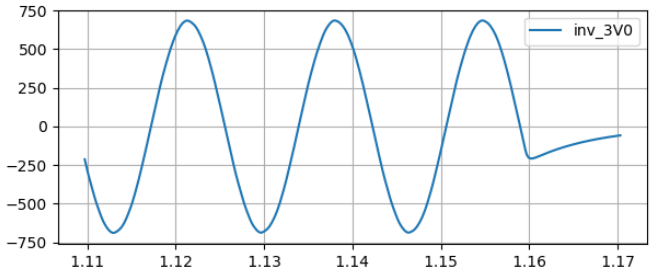

Fig. 19: POI Recorded $3V^{(0)}$ during HIL Testing with Successful Islanding Detection at 1.16 seconds

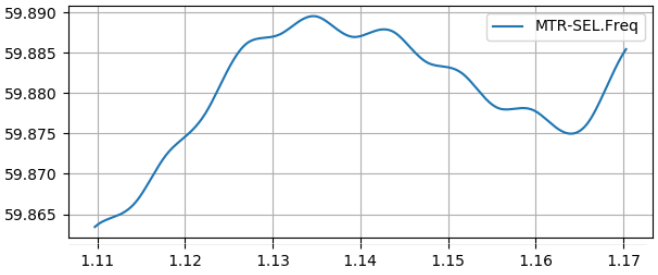

Fig. 20: POI Recorded Frequency during HIL Testing with Successful Islanding Detection at 1.16 seconds

proposed POI schemes proposed in this paper. A local utility was installing a 5MW BESS which was approved as a pilot site for testing. A SEL-651R was installed as the POI protective relay. The one-line for the system is shown in Figure 21.

The settings in the SEL-651R included the settings in Table X in addition to the $3V^{(0)}$ logic and L-L fault detecting logic proposed in Figure(s) 8 and 13.

A. Field Testing: 69kV Transmission LG Fault Event Data

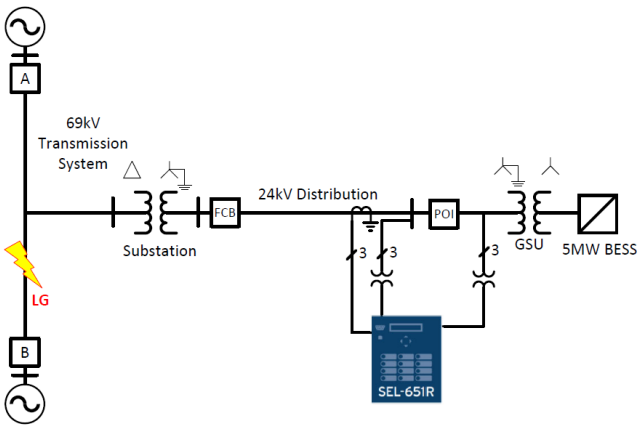

Fig. 21: 69kV Field Test One-Line (SLG Fault on the Transmission System)

At approximately 5AM, a wind-storm caused a tree limb to briefly contact the 69kV Transmission Line. As a result, a SLG fault on the A-Phase at approximately 1 mile from the T/D Step-Down Substation. At the time of the fault, a system operator had dispatched the BESS to 5MW(full rated output). The fault duty was measured at the remote circuit breaker terminals to be around 3600A at Circuit Breaker A and 2900A at Circuit Breaker B.

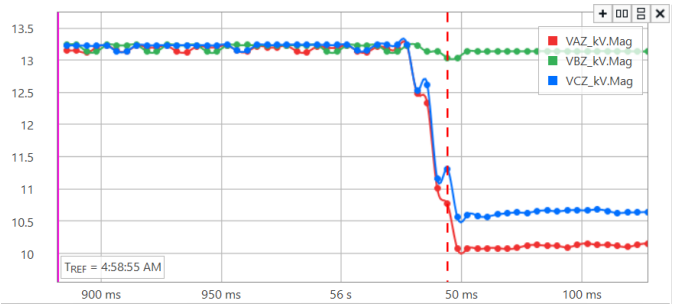

Fig. 22: VA,VB,VC POI oscillography recording during 69kV SLG Fault

It is worth noting that a field visit to the 69kV Circuit Breaker A and B yielded correct targeting(A-G fault). This information was verified by field crews later in the morning as conductor burn marks were used to locate the fault. Although not shown on the SEL-651R events captured, the Transmission Line Circuit Breakers A and B did open and subsequently reclose due to the fault. After the 69kV circuit breakers opened and reclosed, the fault cleared and did not return(1 reclose attempt).

The SEL-651R POI Relaying data was captured below in Figures 22, 23, and 24 to determine if the relaying had properly operated.

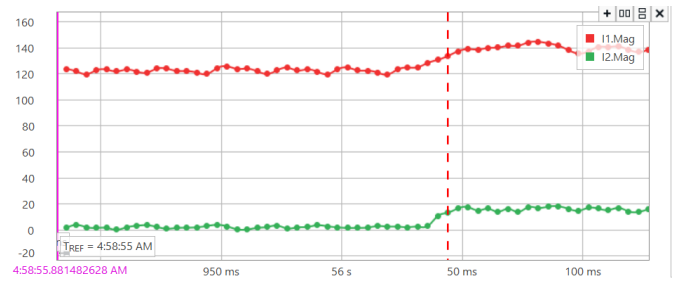

Fig. 23: Negative and Positive Sequence Current Oscillography from IBR during 69kV SLG Fault

Notice in Figure 23 that the inverter acts a constant-power/current limited positive sequence current source(see I1.mag in the Figure). The inverter does inject a very small negative sequence current(I2.mag) due to control loop error. Also, the fault current magnitude of the inverter only increases to approximately 120% of its full output rating.

During the fault, the POI relaying observed the V_{ag} and V_{bg} line-to-ground voltage drop to approximately 10kV, or about 0.75 pu. The variable SV32T was used as a "Transmission Fault detector", and properly targets indicating that a transmission event has occurred. This is shown in Figure 24.

B. Field Testing: 5MW BESS 24kV LG Distribution Fault Event

Several weeks after the initial Transmission fault in the previous section, a Distribution event was recorded. A fuse

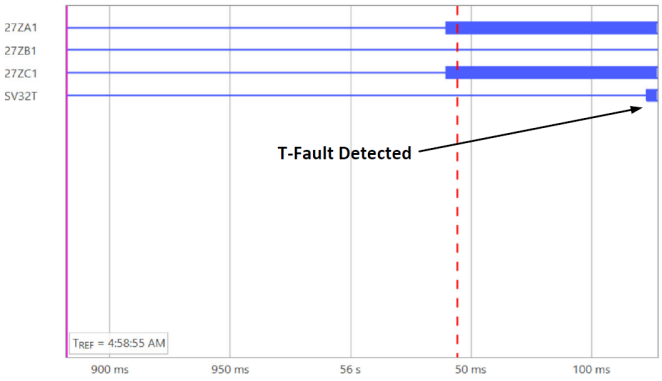

Fig. 24: POI Relay Identifying a Transmission Fault

cutout failure on a 100kVA pole-top single-phase transformer failure resulted in a C-G fault. The fault was located approximately 2 miles from the substation as shown in Figure 25. The approximate distance from the POI was 0.25 miles.

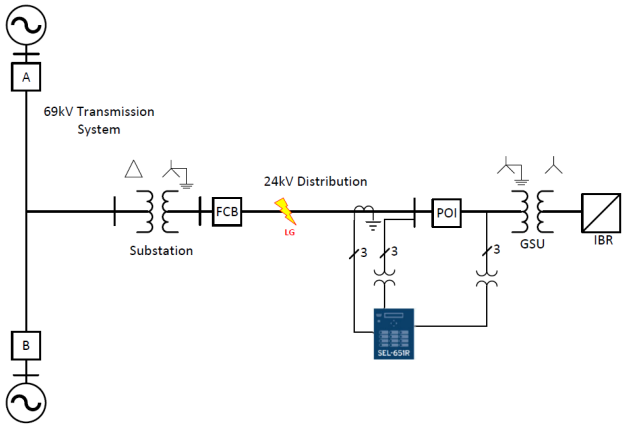

Fig. 25: Field Test One-Line (SLG Fault on the Distribution System)

Although the fault would appear to be permanent, the cutout failure did not manifest as a permanent fault as the cutout split in half during the fault and self-isolated after 1 reclosing attempt. This information was verified by field crews responding to the customer outage.

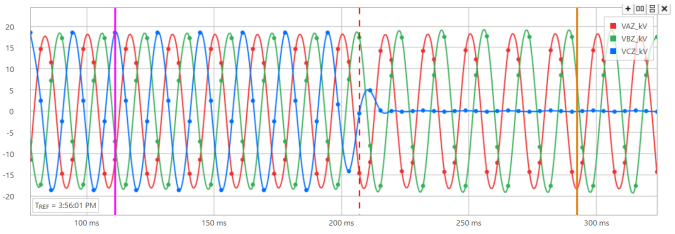

Fig. 26: Phase Voltages(LG) during C-G Fault on Distribution System

After the fault inception, the instantaneous ground overcurrent(set at 2000A with no delay), tripped the Feeder Circuit Breaker. The circuit breaker was set to an open interval of 15 cycles. The POI relaying subsequently observed a large magnitude zero-sequence voltage due to the ground fault and tripped $3V^{(0)}$ Level-2 in 4.5 cycles. The POI relay was able to remove the IBR before the circuit breaker completed Open-Interval timing and subsequent reclosing.

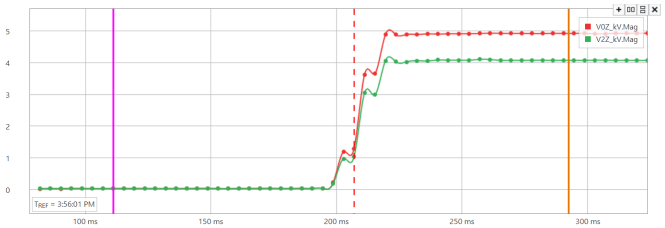

Fig. 27: $V^{(0)}$ and $V^{(2)}$ during C-G Distribution Fault

The voltages observed by the POI are in Figure 26. The sequence voltages, $V^{(0)}$ and $V^{(2)}$ are also shown during the fault in Figure 27. Also, SV24T was used as a Distribution Fault detector, and was used to trip the POI within 4.5 cycles. This is shown in Figure 28.

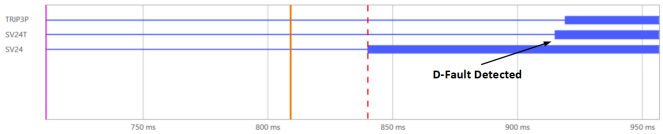

Fig. 28: POI Identifying a Distribution LG Fault

VIII. Conclusion

As a conclusion, Ride-Through does not imply a sacrificing protection speed, selectivity and sensitivity. Techniques proposed in this paper have undergone research and derivation phase, Hardware-in-the-Loop/Laboratory Testing, and pilot testing. Asymmetrical Transmission faults have been shown to be distinguishable from Distribution fault to allow Zone Selective protection(high speed tripping for Distribution faults only). It has also been shown that, despite high islanding risk circuits, Direct Transfer Trip can be avoided. By deploying the novel $3V^{(0)}$ technique, Distribution islanding risk can reduced or even eliminated.

IX. Acknowledgement

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